REMARKS

Claims 6 and 16 are objected to because of language informalities. Claims 10 and 20 are rejected because of language informalities. Claims 1, 2, 5, 6, 8 to 12, 15, 16 and 18 to 20 are rejected under 35 U.S.C. 102(b) as being anticipated by, or in the alternative, under 35 U.S.C. 103(a) as obvious over McCollum et al. (U.S. Patent No. 5,373,169). Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCollum et al. and Go et al. (U.S. Patent No. 5,592,016). Claims 4, 7, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCollum et al. and Cutter et al. (U.S. Patent No. 6,154,410).

1. Objections to claims 6 and 16:

The Markush groupings in Claims 6 and 16 should be put in the proper phrasing, "…selected from the group consisting of…" See MPEP §2173.05(h).

Response:

Claims 6 and 16 are amended in the above AMENDMENT section to contain proper Markush phrasing. Reconsideration of the amended claims 6 and 16 is respectfully requested.

2. Correction of the specification:

The disclosure is objected to because of the following informalities: On Page 6 Paragraph 21 Line 7, "figfig." Should be changed to ---fig.---. Appropriate correction is required.

Response:

The instance of "figfig" is corrected in the above AMENDMENT section as suggested by the examiner. Reconsideration of the corrected specification is respectfully requested.

3. Rejections over claims 10 and 20:

Initially, and with respect to Claims 10 and 20, note that a "product by process" claim is directed to the product per se, no matter how actually made. See *In re Thorpe et al., 227 USPQ 964 (CAFC, 1985)* and the related case law cited therein which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a porduct, whether claimed in "product by process" claims or not. As stated in Thorpe,

> even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown, 459 F.2d 631, 535, 173 USPQ 685, 688 (CCPA 1972); In re Pilkington, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); Buono v. Yankee Maid Dress Corp., 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).*

Note that Applicant has burden of proof in such cases as the above case law makes clear.

Response:

Claims 10 and 20 are cancelled as in the above

AMENDMENT section, and are no longer in need of consideration.

4. Rejections over claims 1, 2, 5, 6, 8 to 12, 15, 16 and 18 to 20 under 35 U.S.C. 102(b) or 103(a):

McCollum et al. show all aspects of the instant invention (e.g. Figure 3c) including:

- a doped amorphous silicon conductive layer 18 set on an isolation layer 20 of a semiconductor wafer 12 and protruding from the surface of the isolation layer
- a dielectric layer made of a bottom oxide layer 24c, a silicon nitride layer 24b and a top oxide layer 24a
- a metal conductive layer 30 set on the surface of the isolation layer and covering the surface of the dielectric layer

As to the grounds of rejection under section 103(a), how the dielectric if fabricated pertains to intermediate process steps and does not affect the final device structure. See MPEP §2113 which discusses the handling of "product by process" claims and recommends the alternative (§102/§103) grounds of rejection.

Response:

Claim 1 is amended as described in the above AMENDMENT section to overcome this rejection. The newly added portion in the amended claim 1 is disclosed in the specification on page 5, paragraph [0021]. No new matter is introduced. The amended claim 1 is repeated below:

"1. (Once amended) An anti-fuse structure having low on-state resistance and low off-state leakage, the anti-fuse structure being set on an isolation layer of a substrate, the structure comprising:

a bottom electrode composed of a silicon conductive layer set in the isolation layer, the silicon conductive layer protruding the surface of the isolation layer;

a dielectric layer set on the top surface of the silicon conductive layer; and

a top electrode composed of a metal conductive layer set on the surface of the isolation layer and covering the surface of the dielectric layer."

As disclosed in the amended claim 1 and Fig. 11 of the present application, the present application provides *a silicon-metal anti-fuse structure 51 including a silicon conductive layer 56 used as a bottom electrode, and a metal conductive layer 66 functioning as a top electrode* of the anti-fuse structure 51 (page 5, paragraph [0021]). In the admitted prior art of the present application, a silicon-silicon anti-fuse structure 11 and a metal-metal anti-fuse structure 31 are introduced as shown in Fig.1 and Fig.2. However, the silicon-silicon anti-fuse structure 11 has a disadvantage of having the high resistance problem, and the metal-metal anti-fuse structure 31 has a disadvantage of having the high current leakage problem (page 3, paragraph [0013]). Therefore, *the present application introduces a new silicon-metal anti-fuse structure to solve the above-mentioned problems*

generated by the silicon-silicon anti-fuse structure and the metal-metal anti-fuse structure. (page 4, paragraph [0016]).

As disclosed in Fig.3C of McCollum et al.'s invention, *McCollum et al. have merely taught a metal-to metal antifuse 40 including a lower electrode composed of a metal layer 14 and a barrier layer 16, and an upper electrode composed of a metal layer 30 and a barrier layer 28* (col. 5, lines 36-37, and 55-56). Although McCollum et al. have mentioned forming an amorphous layer 18, an intermediate antifuse dielectric layer 24, and an amorphous layer 26 on the barrier layer 16, respectively, the amorphous layer 16 is not used as the bottom electrode as taught by the present application. Actually, the amorphous layers 16 and 26 together with the dielectric layer 24 are only used to determine the programming voltage (col. 4, lines 8-10). That is to say, MaCollum et al. possibly disclose a new metal-to-metal antifuse, but not a silicon-metal antifuse as taught by the present application.

For the above-mentioned reasons, the applicant considers that McCollum et al. only disclose the metal-to-metal antifuse as mentioned by the admitted prior art of the present application. Therefore, the applicant believes the amended claim 1 is substantially different from McCollum et al.'s disclosure. Reconsideration of the amended claim 1 is respectively requested.

The amended claim 11 has all of the limitations of

the amended claim 1. Therefore, reconsideration of the amended claim 11 is politely requested.

Claims 10 and 20 are cancelled. The rejected claims 2, 5, 8-9 and amended claim 6 are dependent on claim 1 and should be allowed if the amended claim 1 is allowed. Likewise, the rejected claims 12, 15, 17-18 and amended claim 16 are dependent on claim 11 and should be allowed if the amended claim 11 is allowed. Reconsideration of the rejections over claims 2, 5, 6, 8-10, 12, 15, 16, and 18-20 is therefore requested.

5. Rejections over claims 3 and 13 under 35 U.S.C. 103(a):

McCollum et al. show most aspects of the instant invention (Paragraph 6) except for the SOI substrate. Go et al. teach (e.g. Figure 14) is common and, therefore obvious, to one of ordinary skill in the art to form anti-fuse structures 210 on SOI substrates 12, 14.

Response:

The rejected claim 3 is dependent on claim 1 and should be allowed if the amended claim 1 is allowed. Likewise, the rejected claim 13 is dependent on claim 11 and should be allowed if the amended claim 11 is allowed. Reconsideration of the rejections over claims 3 and 13 is therefore requested.

6. Rejection over claims 4, 7, 14 and 17 under 35 U.S.C. 103(a):

McCollum et al. show most aspects of the instant invention (Paragraph 6) except for the silicon

conductive layer made of doped polysilicon and the surface of the silicon conductive layer having HSG structures. Cutter et al. teach (e.g. Figure 3) to use polysilicon layer having HSG structures 22 in anti-fuse 40 to increase programming speed (Column 3 Lines 48 to 59). Although not explicitly stated, it would be obvious to doped the polysilicon layer to further increase the conductivity and the speed of the programming. It would have been obvious to a person of ordinary skill in the art at the time of invention to use doped polysilicon layer having HSG structures as taught by Cutter et al. in the anti-fuse of McCollum et al. to increase programming speed.

Response:

The rejected claims 4 and 7 are dependent on claim 1 and should be allowed if the amended claim 1 is allowed. Likewise, the rejected claims 14 and 17 are dependent on claim 11 and should be allowed if the amended claim 11 is allowed. Reconsideration of the rejections over claims 4, 7, 14 and 17 is therefore requested.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification:

1. Page 5, paragraph [0021], line 7: replace "Fig.Fig." with ---Fig.---.

In the claims:

1. (Once amended) An anti-fuse structure having low on-state resistance and low off-state leakage, the anti-fuse structure being set on an isolation layer of a substrate, the structure comprising:

a bottom electrode composed of a silicon conductive layer set in the isolation layer, the silicon conductive layer protruding the surface of the isolation layer;

a dielectric layer set on the top surface of the silicon conductive layer; and

a top electrode composed of a metal conductive layer set on the surface of the isolation layer and covering the surface of the dielectric layer.

6. (Once amended) The structure of claim 1 wherein the silicon conductive layer [comprises]is selected from the group consisting of doped polysilicon, doped amorphous silicon [or]and silicide.

Claim 10 is cancelled.

11. (Once amended) An anti-fuse structure, the structure comprising:

a bottom electrode composed of a silicon conductive layer;

a dielectric layer set on the surface of the silicon

conductive layer; and

an top electrode composed of a metal conductive layer covering the surface of the dielectric layer.

16. (Once amended) The structure of claim 11 wherein the silicon conductive layer [comprises] is selected from the group consisting of doped polysilicon, doped amorphous silicon [or] and silicide.

Claim 20 is cancelled.

Sincerely yours,

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